



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,287	07/18/2003	Rahul Saxena	P16855	4600
50890	7590	04/30/2008		
CAVEN & AGHEVLI c/o INTELLEVATE, LLC P.O. BOX 52050 MINNEAPOLIS, MN 55402				
EXAMINER				
HUSSAIN, TAUQIR				
ART UNIT		PAPER NUMBER		
2152				
MAIL DATE		DELIVERY MODE		
04/30/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/622,287

Applicant(s)

SAXENA, RAHUL

Examiner

TAUQIR HUSSAIN

Art Unit

2152

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02/11/2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 4, 5, 7-19, 21 and 23-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 4-5, 7-19, 21, 23-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF-08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/11/2008 has been entered.

Response to Amendment

2. This office action is in response to amendment /reconsideration filed on 02/11/2008, the amendment/reconsideration has been considered. Claims 3, 6, 20 and 22 have been cancelled and therefore, claims 1, 2, 4, 5, 7-19, 21, 23-30 are pending for examination, the rejection cited as stated below.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
4. Claims 1, 2, 4, 5, 7-19, 21 and 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viswanath et al. (Patent Number: 6151322), hereinafter "Viswanath" in view of Brukert et al (Patent No.: US 4916704 A), hereinafter "Brukert".
5. As to claim 1, Viswanath discloses, a method of operating a network device, comprising:

receiving electronic data from a first port of the data networking device (Abstract, lines 1-2);

discarding at least a portion of the electronic data prior to providing the electronic data to a memory of the networking device Abstract, lines 3-10, where stripping the tag means discard the portion of the electronic data and Col.7, lines 10-13, where VLAN tag is extracted means discarded and only VLAN ID is stored with frame in a memory);

providing at least a portion of the electronic data to a second port (Abstract, lines 16-20, where transmitting port is the second port).

generating a code and inserting the code into the frame prior to providing to the memory (Fig.4, Elements-84 and 64, Col.7, lines 21-39, where tagging can be interpreted as coding and modifying means adding or deleting or inserting the appropriate information into frame and sending it to memory 64).

Viswanath however is silent on disclosing generating CRC and inserting CRC into a frame.

Brkert however discloses, generating CRC and inserting CRC into a frame (Col.21, lines 20-28, where CRC generator generates the CRC and checks the same CRC code that is used by I/O device before further processing of sending it to network port or disk interface which can also be interpreted as memory).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to combine the teachings of Viswanath with the CRC concept disclosed in Brkert in order to provide a provide a fault tolerant computer method and system having duplicate computer systems which normally operate

Art Unit: 2152

simultaneously. The duplication insures that there is no single point of failure and an error or fault in one of the systems will not disable the overall computer system.

1. As to claim 10, an apparatus, comprising:

one or more receive ports capable of receiving electronic data from a network
(Col.7, liens 10-11, where switch receiving packets on one of the ports);

one or more transmit ports capable of transmitting electronic data to a network
(Col.7, lines 42-44);

a memory (Col.7, lines 12-13; and

a processor, the processor configured to, in operation (Fig.3, Element-70):

discard at least a portion of the electronic data received by the one or more
receive ports (and Col.7, lines 10-13, where VLAN tag is extracted means discarded
and only VLAN ID is stored with frame in a memory);

provide the remaining electronic data to the memory (Col.7, line 13);

read the electronic data from the memory (Col.7, lines 17-18);

modify the electronic data after reading from the memory (Col.7, lines 32-33);

and

provide at least a portion of the electronic data to one or more of the transmit
ports (Col.7, lines 42-44).

wherein the electronic data is to comprise a frame and wherein the processor is
to cause generation of a code and insertion of the code into the frame prior to storage in
the memory (Fig.4, Elements-84 and 64, Col.7, lines 21-39, where tagging can be

interpret as coding and modifying means adding or deleting or inserting the appropriate information into frame and sending it to memory 64).

Viswanath however is silent on disclosing explicitly, "generation of a CRC (Cyclic redundancy code) and insertion of the CRC into the frame".

Brkert however discloses, generating CRC and inserting CRC into a frame (Col.21, lines 20-28, where CRC generator generates the CRC and checks the same CRC code that is used by I/O device before further processing of sending it to network port or disk interface which can also be interpret as memory).

2. Claim 19, carry similar limitation as claim 1 and 10 above and therefore, is rejected under for same rationale.
3. As to claim 2, Viswanath and Brkert disclose the invention substantially as in parent claim 1 above, including, modifying the electronic data prior to said providing (Viswanath, Abstract, lines 3-5, where striping is modifying).
4. As to claims 4 and 14, Viswanath and Brkert disclose the invention substantially as in parent claims 1 and 10 above, including, wherein the portion of electronic data deleted comprises a VLAN (virtual local area network) tag (Viswanath, Abstract, line 3).
5. As to claim 5, Viswanath and Brkert disclose the invention substantially as in parent claim 1 above, including, wherein modifying comprises inserting a VLAN tag to the frame (Viswanath, Abstract, lines 14-16).

6. As to claim 7, Viswanath discloses, providing a portion of the electronic data to a control module prior to deleting a portion of the electronic data (Viswanath, Fig.4, Elements-84 and 64, Col.7, lines 17-21, where comparator 84 is control module, lines 32-33, where data is modified means deleting or adding header information and lines 37-39, where data is transferred to element-64, which is memory).

7. As to claim 8, Viswanath and Brukert disclose the invention substantially as in parent claim 7 above, including, wherein the portion of data provided to the control module comprises the protocol header (Viswanath, Fig.1a and 1b, Col.3, lines 31-33, Inherently protocol header is there, e.g. VLAN type, source address, destination address etc.).

8. As to claim 9, Viswanath discloses, wherein the first port and the second port comprise a receive port and a transmit port, respectively (Viswanath, Col.7, lines 10, where receiving port could be first port and lines 42-44, where output port is transmit port).

9. As to claim 11, Viswanath and Brukert disclose the invention substantially as in parent claim 10 above, including, wherein the processor is further configured to modify the electronic data prior to providing at least a portion of the electronic data to one or more of the transmit ports (Viswanath, Col.7, lines 42-44, where out put port is transmit port and VLAN insertion means the data has been modified).

10. As to claim 12, Viswanath and Brukert disclose the invention substantially as in parent claim 1 above, including, wherein the apparatus comprises a network switch (Viswanath, Fig.2, Col.7, lines 10-11, where network switch means apparatus).

11. As to claim 13, Viswanath and Brukert disclose the invention substantially as in parent claim 12 above, including, wherein said memory comprises network switch internal memory (Viswanath, Fig.4, Element-64 and 80).

12. As to claim 15, Viswanath and Brukert disclose the invention substantially as in parent claim 11 above, including, wherein modifying the electronic data comprises inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination address of the electronic data (Viswanath, Col.7, lines 42-44, where VLAN tag is inserted as a destination address).

13. As to claim 16, Viswanath and Brukert disclose the invention substantially as in parent claim 10 above, including, wherein the processor comprises a network processor (Viswanath, Fig.3b, Element-70, Col.6, lines 25-26, where network switch has decision making engine which is processor and since switch is a network device therefore, processor is a network processor).

14. As to claim 17, Viswanath and Brukert disclose the invention substantially as in parent claim 10 above, including, wherein the memory comprises a plurality of memory devices (Viswanath, Fig.3b, and Elements-32, 64 and 66, Col.5, lines 50-51 and 56).

Art Unit: 2152

15. As to claim 18, Viswanath and Brukert disclose the invention substantially as in parent claim 17 above, including, wherein the plurality of memory devices comprise one or more of:

random access memory (Viswanath, Col.7, line 62) and

synchronous dynamic random access memory (Viswanath, Col.5, lines 7-9).

16. Claims 20-26 are rejected for the same reasons as applied above to claims 5, 4, 6 and 15-18 respectively.

17. As to claim 27, Viswanath and Brukert disclose the invention substantially as in parent claim 19 above, including, wherein said processor is configured to modify said electronic data only if said second port is configured to recognize tags (Viswanath, Col.7, lines 10-13, where processor processes the tagged packets and lines 42-45, transmitted to VLAN ports which means there are out put ports configured to handle tagged packets).

18. As to claim 28, Viswanath and Brukert disclose the invention substantially as in parent claim 10 above, including, further comprising, the processor is to generate a CRC of a non-discarded portion of the electronic data (Viswanath, Fig.4 Col.7, lines 10-29, where inherently destination tag is generated for the frame and not for the striped tag)

19. Claims 29-30 has same limitations as of claim 28 and therefore, are rejected for same rationale as applied to claim 28 above.

6. **Examiner's Note:** Examiner has cited particular columns and line numbers in the references, as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in its entirety as potentially teaching of all or part of the claimed invention, as well as the context.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TAUQIR HUSSAIN whose telephone number is (571)270-1247. The examiner can normally be reached on 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571 272 3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2152

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/T. H./

Examiner, Art Unit 2152

/Bunjod Jaroenchonwanit/

Supervisory Patent Examiner, Art Unit 2152